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EXAMINER	
PIZIALI, JEFFREY J	
ART UNIT	PAPER NUMBER
2629	

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Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Office Action Summary	Application No.	Applicant(s)	
	10/714,216	HATTI ET AL.	
	Examiner	Art Unit	
	JEFF PIZIALI	2629	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE *3* MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *17 November 2009*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *8,9,11-14 and 21* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *8,9,11-14 and 21* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☒ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *14 November 2003* is/are: a)☐ accepted or b)☒ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

DETAILED ACTION

Priority

1. Receipt is acknowledged of papers submitted under 35 U.S.C. 119(a)-(d), which papers have been placed of record in the file.

Drawings

2. The drawings are objected to as failing to comply with 37 CFR 1.84(p)(5) because they include the following reference character(s) not mentioned in the description: "L_0, L_1,... L_x L_{x+1}, L_N" (see Fig. 1); ***"Video Signal Encoder 55"*** (see Fig. 3); and ***"835a-835f"*** (see Fig. 5).

Corrected drawing sheets in compliance with 37 CFR 1.121(d), or amendment to the specification to add the reference character(s) in the description in compliance with 37 CFR 1.121(b) are required in reply to the Office action to avoid abandonment of the application. Any amended replacement drawing sheet should include all of the figures appearing on the immediate prior version of the sheet, even if only one figure is being amended. Each drawing sheet submitted after the filing date of an application must be labeled in the top margin as either "Replacement Sheet" or "New Sheet" pursuant to 37 CFR 1.121(d). If the changes are not accepted by the examiner, the applicant will be notified and informed of any required corrective action in the next Office action. The objection to the drawings will not be held in abeyance.

3. The drawings have not been checked to the extent necessary to determine the presence of all possible minor errors. Applicant's cooperation is requested in correcting any errors of which applicant may become aware in the figures.

Specification

4. The disclosure is objected to because of the following informalities:

The term "***means of a vertical synchronization pulses***" should be corrected (*page 1, paragraph 4, line 5*).

Appropriate correction is required.

5. The specification has not been checked to the extent necessary to determine the presence of all possible minor errors. Applicant's cooperation is requested in correcting any errors of which applicant may become aware in the specification.

Claim Rejections - 35 USC § 112

6. The following is a quotation of the second paragraph of 35 U.S.C. 112:

> The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.

7. *Claims 8, 9, 11-14, and 21* are rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention.

8. Claim 8 is rejected under 35 U.S.C. 112, second paragraph, as being incomplete for omitting essential structural cooperative relationships of elements, such omission amounting to a gap between the necessary structural connections. See MPEP § 2172.01.

An omitted structural cooperative relationship results from the claimed subject matter: "***a rasterizing circuit for rasterizing a first frame***" (*line 2*) and "***after the rasterizing circuit provides the first frame***" (*line 4*).

It would be unclear to one having ordinary skill in the art whether the limitations of "***rasterizing a first frame***" and "***provides the first frame***" are intended to be identical to, or distinct from, one another.

The Applicant is respectfully requested to clarify whether "***providing the first frame***" is a distinct function/operation; or rather explain if "***provides the first frame***" in inherent when "***rasterizing a first frame***."

9. Claim 8 recites the limitation "***after the rasterizing circuit provides the first frame***" (*line 4*). There is insufficient antecedent basis for this limitation in the claim.

It would be unclear to one having ordinary skill in the art what antecedent basis exists in the claim for, "***the rasterizing circuit provides the first frame***."

10. The remaining claims are rejected under 35 U.S.C. 112, second paragraph, as being dependent upon rejected base claims.

11. The claims are rejected under 35 U.S.C. 112, second paragraph, as being indefinite.

As a courtesy to the Applicant, the examiner has attempted to also make rejections over prior art -- based on the examiner's best guess interpretations of the invention that the Applicant is intending to claim.

However, the indefinite nature of the claimed subject matter naturally hinders the Office's ability to search and examine the application.

Any instantly distinguishing features and subject matter that the Applicant considers to be absent from the cited prior art is more than likely a result of the indefinite nature of the claims.

The Applicant is respectfully requested to correct the indefinite nature of the claims, which should going forward result in a more precise search and examination.

Claim Rejections - 35 USC § 102

12. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

13. Claims *8, 9, and 11-14* are rejected under 35 U.S.C. 102(b) as being anticipated by ***Sotheran (US 5,603,012 A)***.

Regarding claim 8, ***Sotheran*** discloses a system for displaying frames, said system comprising:

a rasterizing circuit [*e.g., 3-buffer system, READY buffer*] for rasterizing [*e.g., converts picture/image data into pixels*] a first frame [*e.g., a first, previous frame of picture data*]

(*see the entire document, including Column 325, Lines 55-61*);

a controller [*e.g., buffer manager*] for providing information [*e.g., status information -- e.g., buffer flagged as READY*] regarding a second frame [*e.g., a second, next, new frame of picture data following the first frame of picture data*] to the rasterizing circuit,

after the rasterizing circuit provides the first frame; and wherein

the rasterizing circuit rasterizes the first frame [*e.g., previous displayed buffer frame picture is repeated*],

if the controller does not provide the information [*e.g., buffer not flagged as READY*] regarding the second frame to the rasterizing circuit before a first horizontal synchronization pulse [*e.g., hsync*] following a vertical synchronization pulse [*e.g., vsync*] associated with the second frame

(*see the entire document, including Column 295, Line 45 - Column 296, Line 40*).

Sotheran explains, "*The display address generator requests a new display buffer,* ***once every vsync****, via a two-wire interface. If there is a* ***buffer flagged as READY, then that will be allocated to display by the buffer manager****. If there is* ***no READY buffer, the previously displayed buffer will be repeated***" (*see Column 296, Lines 17-21*).

Therefore, ***Sotheran*** teaches not providing the information [*e.g., buffer not flagged as READY*] regarding the second frame to the display engine following a vertical synchronization pulse [*e.g., wherein vsync for the first frame and second frame are both "associated" -- in different ways -- with the second frame*].

Sotheran also goes on to define '*vdelay*' as "*The* ***number of hsync pulses following a vsync pulse*** *before the first line of video or border... The minimum vdelay is zero.* ***The first hsync is the first active line***" (see Column 333, Lines 48-59).

As such, ***Sotheran*** clearly teaches at least one first horizontal synchronization pulse [*e.g., hsync*] following a vertical synchronization pulse [*e.g., vsync*].

Therefore, if ***Sotheran's*** (READY or NOT-READY) buffer status check occurs *during* the vertical synchronization pulse (*as taught by* ***Sotheran*** *at Column 296, Lines 17-21; and as further acknowledged by the Applicant at Page 4, Line 25 of the* ***Response*** *filed on 17 November 2009*), and

the first horizontal synchronization pulse occurs *after* the vertical synchronization pulse (*as taught by* ***Sotheran*** *at Column 333, Lines 48-59; and as further taught by Figure 1 and Paragraphs 4-7 of the instant application's own* ***Background of the Invention***),

then the (READY or NOT-READY) buffer status check must occur *before* the first horizontal synchronization pulse, as instantly claimed.

Regarding claim 9, ***Sotheran*** discloses the rasterizing circuit rasterizes the second frame [*e.g., converts the second, next, new frame of picture data following the first frame of picture data into pixels*] if the controller provides the information regarding the second frame [*e.g., status information -- e.g., buffer flagged as READY*] before the first horizontal synchronization pulse following the vertical synchronization pulse associated with the second frame (*see the entire document, including Column 295, Line 45 - Column 296, Line 40*).

Sotheran explains, "*If there is a* ***buffer flagged as READY, then that will be allocated to display by the buffer manager***." (*see Column 296, Lines 17-21*).

Regarding claim 11, ***Sotheran*** discloses a frame buffer [*e.g., three buffers*] for storing the second frame beginning at at least one starting address [*e.g., buffer flagged as READY*]; and wherein

the information regarding the second frame comprises the at least one starting address (*see the entire document, including Column 295, Line 45 - Column 296, Line 40*).

Regarding claim 12, ***Sotheran*** discloses a first at least one register [*e.g., three buffers*] for storing information regarding the first frame (*see the entire document, including Column 295, Line 45 - Column 296, Line 40*).

Regarding claim 13, ***Sotheran*** discloses the rasterizing circuit rasterizes the first frame based [*e.g., converts first, previous frame of picture data into pixels*] on the information regarding the first frame if the controller does not provide the information [*e.g., buffer not flagged as READY*] regarding the second frame before the first horizontal synchronization pulse following the vertical synchronization pulse associated with the second frame (*see the entire document, including Column 295, Line 45 - Column 296, Line 40*).

Regarding claim 14, ***Sotheran*** discloses the controller overwrites [*e.g., EMPTY buffer*] the information regarding the first frame with the information regarding the second frame and

wherein the rasterizing circuit rasterizes the second frame based on the information regarding the second frame (*see the entire document, including Column 295, Line 45 - Column 296, Line 40*).

Claim Rejections - 35 USC § 102 / 103

14. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

15. *Claim 21* is rejected under 35 U.S.C. 102(b) as anticipated by ***Sotheran (US 5,603,012 A)***; or, in the alternative, under 35 U.S.C. 103(a) as obvious over ***Sotheran (US 5,603,012 A)*** in view of the instant ***Application's Admitted Prior Art (AAPA)***.

Regarding claim 21, ***Sotheran*** discloses the rasterizing circuit rasterizes the second frame [*e.g., converts the second, next, new frame of picture data following the first frame of picture data into pixels*],

if the controller provides the information regarding the second frame [*e.g., status information -- e.g., buffer flagged as READY*] to the rasterizing circuit after the vertical synchronization pulse [*e.g., the start of vsync*] associated with the second frame and

before the first horizontal synchronization pulse [*e.g., hsync*] following the vertical synchronization pulse associated with the second frame

(*see the entire document, including Column 295, Line 45 - Column 296, Line 40*).

Should it be shown that ***Sotheran*** teaches the claimed "*after the vertical synchronization pulse and before the first horizontal synchronization pulse*" subject matter with insufficient specificity:

The ***AAPA*** discloses that it is conventional in the field of display devices that, "*between the vertical synchronization pulse [Fig. 1: $Vsynch_0$] and the first horizontal synchronization pulse [Fig. 1: $Hsynch_0$], there is a period of time known as the vertical blanking interval [Fig. 1: VBI].*"

Furthermore, the ***AAPA*** discloses, "*during the VBI, preparations are made for displaying the next frame*" (*see the entire **AAPA**, including Paragraphs 4-6*).

Sotheran and the ***AAPA*** are analogous art, because they are from the shared inventive field of providing synchronized frames to a display device.

Therefore, it would have been obvious to one having ordinary skill in the art to perform ***Sotheran's*** (READY or NOT-READY) buffer status check during the vertical blanking interval between the vertical and horizontal synchronization pulses, so as to make use of a well known and commonly understood time interval for making incoming display-frame preparations.

It would have been obvious to one of ordinary skill in the art at the time of invention, because the substitution of one known *vertical blanking frame preparation interval* for another *vertical synchronization pulse frame preparation interval* would have yielded predictable results to one of ordinary skill in the art at the time of the invention.

Response to Arguments

16. Applicant's arguments filed on *17 November 2009* have been fully considered but they are not persuasive.

The Applicant contends, "*Assignee respectfully traverses the rejection, because although* ***Sotheran*** *teaches that 'display address generator requests a new display buffer, one every vsync',* ***Sotheran*** *does not indicate when during the vsync such request is made. More particularly,* ***Sotheran*** *does not teach that the foregoing occurs either before or after vsync + vdelay. Thus,* ***Sotheran*** *does not teach 'wherein the rasterizing circuit rasterizes the first frame, if the controller does not provide the information regarding the second frame to the display engine before a first horizontal synchronization pulse following a vertical synchronization pulse associated with the second frame'* " (see Page 4 of the Response filed on *17 November 2009*). However, the examiner respectfully disagrees.

Firstly, as the applicant notes above, ***Sotheran*** teaches, "*The display address generator requests a new display buffer,* ***once every vsync****, via a two-wire interface. If there is a* ***buffer flagged as READY, then that will be allocated to display by the buffer manager****. If there is* ***no READY buffer, the previously displayed buffer will be repeated***" (*see Column 296, Lines 17-21*).

The applicant alleges, "***Sotheran*** *does not indicate when during the vsync such request is made*" (see Page 4, Line 25 of the Response filed on *17 November 2009*) -- thereby

acknowledging that the (READY or NOT-READY) buffer status check occurs *during the vertical synchronization pulse*.

Secondly, ***Sotheran*** teaches that the first horizontal synchronization pulse of an image frame occurs *after* the vertical synchronization pulse of the frame (see Column 333, Lines 48-59).

Thirdly, the instant application's own ***Background of the Invention*** teaches that it is conventional for the first horizontal synchronization pulse [*Fig. 1: $Hsynch_0$*] of an image frame [*Fig. 1: Frame 100_0*] to occur *after* the vertical synchronization pulse [*Fig. 1: $Vsynch_0$*] of the frame (*see Paragraphs 4-7*)

Therefore, if the (READY or NOT-READY) buffer status check occurs *during* the vertical synchronization pulse, and

the first horizontal synchronization pulse occurs *after* the vertical synchronization pulse,

then the (READY or NOT-READY) buffer status check must occur *before* the first horizontal synchronization pulse.

The Applicant contends, "***Sotheran*** *at col. 295, line 45 - column 296, line 40, clearly does not teach or fairly suggest 'wherein the rasterizing circuit rasterizes the second frame, if the controller provides the information regarding the second frame to the rasterizing circuit after the vertical synchronization pulse associated with the second frame and before a first horizontal*

synchronization pulse following a vertical synchronization pulse associated with the second frame'. Note that 'rasterizes the second frame, if the controller provides the information ... after the vertical synchronization pulse and before a first horizontal synchronization pulse following a vertical synchronization pulse', is in contrast with 'requests a new display buffer, once very vsync .... If there is no READY Buffer, the previously displayed buffer will be repeated' " (see Page 5 of the Response filed on *17 November 2009*). However, the examiner respectfully disagrees.

Sotheran discloses the rasterizing circuit rasterizes the second frame [*e.g., converts the second, next, new frame of picture data following the first frame of picture data into pixels*],

if the controller provides the information regarding the second frame [*e.g., status information -- e.g., buffer flagged as READY*] to the rasterizing circuit after the vertical synchronization pulse [*e.g., the start of vsync*] associated with the second frame and

before the first horizontal synchronization pulse [*e.g., hsync*] following the vertical synchronization pulse associated with the second frame

(*see the entire document, including Column 295, Line 45 - Column 296, Line 40*).

Applicant's arguments with respect to *claims 8, 9, 11-14, and 21* have been considered but are moot in view of the new ground(s) of rejection.

By such reasoning, rejection of the claims is deemed necessary, proper, and thereby maintained at this time.

Conclusion

17. Applicant's amendment necessitated the new ground(s) of rejection presented in this Office action. Accordingly, **THIS ACTION IS MADE FINAL**. See MPEP § 706.07(a). Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the date of this final action.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Jeff Piziali whose telephone number is (571) 272-7678. The examiner can normally be reached on Monday - Friday (6:30AM - 3PM).

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Chanh Nguyen can be reached on (571) 272-7772. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

/Jeff Piziali/
Primary Examiner, Art Unit 2629
3 February 2010